DESCRIPTION

The SN74LVC1G3157 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay while maintaining CMOS low power dissipation. Analog and digital voltages that may vary across the full power−supply range (from VCC to GND).

The Select pin has over voltage protection that allows voltages above VCC , up to 7.0 V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

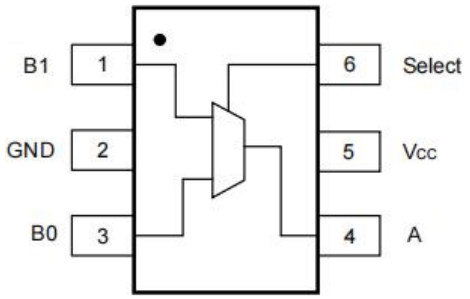
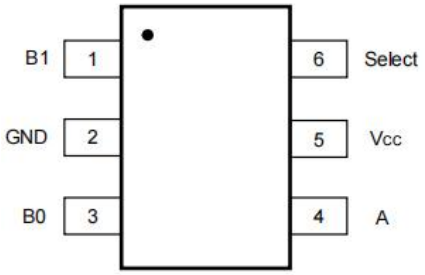
FEATURES

- Low power dissipation
- High speed
- Standard CMOS logic levels
- High bandwidth, improved linearity
- Switches Standard NTSC/PAL Video, Audio, SPDIF and HDTV
- be used for Clock Switching, Data Mux'ing,etc.
- Low RDSON
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- Operating temperature -40C ~ +85C
- package : SC70-6, SOT23-6

ORDER INFORMATION

P/N	PKG	QTY
SN74LVC1G3157DCKR	SC70-6	Tape and Reel, 3000
SN74LVC1G3157DBVR	SOT23-6	Tape and Reel, 3000

PIN CONFIGURATION (Top View)

SC70-6	SOT23-6
	

PIN DESCRIPTIONS

Pin	I/O	Pin Function
A, B0 , B1	I/O	Data port
Select	I	Controlling choice
VCC	/	Power supply port
GND	/	Ground

FUNCTIONS DESCRIPTION

Select input port	Function
L	B0 Connected to A
H	B1 Connected to A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 ~ +7.0	V
DC Switch Voltage (1)	V_S	-0.5 ~ V_{CC}+0.5	V
DC Input Voltage (1)	V_{IN}	-0.5 ~ +7.0	V
DC Input Diode Current @ V_{IN} < 0 V	I_{IK}	-50	mA
DC Output Current	Iout	128	mA
DC V_{CC} or Ground Current	Icc/I_{GND}	100	mA
Storage Temperature Range	Tstg	-65 ~ +150	C
Junction Temperature Under Bias	T_J	150	C
Junction Lead Temperature (Soldering, 10 Seconds)	T_L	260	C
Power Dissipation @ +85°C	P_D	180	mW

NOTE:

Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. QCSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

QCSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDITIONS (2)

Characteristic		Symbol	Min	Max	Unit
Supply Voltage Operating		VCC	1.65	5.5	V
Select Input Voltage		VIN	0	VCC	V
Switch Input Voltage		VIN	0	VCC	V
Output Voltage		VOUT	0	VCC	V
Operating Temperature		TA	-55	+125	C
Input Rise and Fall Time	Control Input VCC = 2.3 V ~ 3.6 V	tr,tf	0	10	ns/V
	Control Input VCC = 4.5 V ~ 5.5 V		0	5.0	

Note:

2. Select input must be held HIGH or LOW, it must not float.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	VCC	T_A = 25C			T_A = -40C ~ +85C		Unit
				Min	Typ	Max	Min	Max	
DC ELECTRICAL CHARACTERISTICS									
V_{IH}	High Level Input Voltage		1.65 ~ 1.95				0.75Vcc		V
			2.3 ~ 2.8				1.5		
			3 ~ 4.2				2.4		
			4.5 ~ 5.5				0.6Vcc		
V_{IL}	Low Level Input Voltage		1.65 ~ 1.95					0.25VCC	V
			2.3 ~ 2.8					0.4	
			3 ~ 5.5					0.3Vcc	
I_{IN}	Input Leakage Current	0 < V_{IN} < 5.5 V	0 ~ 5.5		±0.05	±0. 1		±1	uA
I_{OFF}	OFF State Leakage Current	0 < A, B < Vcc	1.65 ~ 5.5		±0.05	±0. 1		±1	uA
I_{CC}	Quiescent Supply	V_{IN} = Vcc or GND I_{OUT} = 0	5.5			1.0		10	uA
	Analog Signal Range		VCC	0		VCC	0	VCC	V
RON	Switch On Resistance(3)	V_{IN} = 0 V, I_O = 30 mA	4.5		3.0			7.0	Ω
		V_{IN} = 2.4 V, I_O = -30 mA			5.0			12	Ω
		V_{IN} = 4.5 V, I_O = -30 mA			7.0			15	Ω
		V_{IN} = 0 V, I_O = 24 mA	3.0		4.0			9.0	Ω
		V_{IN} = 3 V , I_O = -24 mA			10			20	Ω
		V_{IN} = 0 V, I_O = 8 mA	2.3		5.0			12	Ω
		V_{IN} = 2.3 V, I_O = -8 mA			13			30	Ω
		V_{IN}=0V, I_O =4 mA	1.65		6.5			20	Ω
		V_{IN} = 1.65 V, I_O = -4 mA			17			50	Ω
RRANGE	On Resistance Over Signal Range(3)(7)	I_A = -30 mA 0 ≤ V_{Bn} ≤ VCC	4.5					25	Ω
		I_A = -24 mA 0 ≤ V_{Bn} ≤ VCC	3					50	Ω

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	VCC	TA = 25C			TA = -40C ~ +85C		Unit
				Min	Typ	Max	Min	Max	
RRANGE	On Resistance Over Signal Range(3)(7)	IA = -8 mA 0 ≤ VBn ≤ VCC	2.3					100	Ω
		IA = -4 mA 0 ≤ VBn ≤ VCC	1.65					300	Ω
Δ RON	On Resistance Match Between Channels(3)(4)(5)	IA = -30 mA VBn = 3.15	4.5		0.15				Ω
		IA = -24 mA VBn = 2.1	3		0.2				Ω
		IA = -8 mA VBn = 1.6	2.3		0.5				Ω
		IA = -4 mA VBn = 1.15	1.65		0.5				Ω
RFLAT	On Resistance Flatness(3)(4)(6)	IA = -30 mA 0 ≤ VBn ≤ VCC	5		6.0				Ω
		IA = -24 mA 0 ≤ VBn ≤ VCC	3.3		12				Ω
		IA = -8 mA 0 ≤ VBn ≤ VCC	2.5		28				Ω
		IA = -4 mA 0 ≤ VBn≤ VCC	1.8		125				Ω
AC ELECTRICAL CHARACTERISTICS									
tPHL tPLH	Propagation Delay Bus to Bus (8)	Figure 1 VI = OPEN	1.65 ~ 1.95						nS
			2.3 ~ 2.7					1.2	nS
			3.0 ~ 3.5					0.8	nS
			4.5 ~ 5.5					0.3	nS
tPZL tPZH	Output Enable Time, Turn On Time (A to Bn)	Figure 1 VI = 2*VCC for tPZL ,VI = 0 V for tPZH	1.65 ~ 1.95			23	7.0	24	nS
			2.3 ~ 2.7			13	3.5	14	nS
			3.0 ~ 3.5			6.9	2.5	7.6	nS
			4.5 ~ 5.5			5.2	1.7	5.7	nS
tPLZ tPHZ	Output Disable Time, Turn Off Time (A Port to B Port)	Figure 1 VI = 2*VCC for tPLZ ,VI = 0 V for tPHZ	1.65 ~ 1.95			12.5	3.0	13	nS
			2.3 ~ 2.7			7.0	2.0	7.5	nS
			3.0 ~ 3.5			5.0	1.5	5.3	nS
			4.5 ~ 5.5			3.5	0.8	3.8	nS

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	VCC	T_A = 25°C			T_A = -40°C ~ +85°C		Unit
				Min	Typ	Max	Min	Max	
tB-M	Break Before Make Time (7)	Figure2 , C_L = 50 pF , R_L = 600 Ω	1.65 ~ 1.95				0.5		nS
			2.3 ~ 2.7				0.5		nS
			3.0 ~ 3.5				0.5		nS
			4.5 ~ 5.5				0.5		nS
Q	(7) Charge Injection	Figure 3, C_L = 0.1 nF , V_{GEN} = 0 V , R_{GEN} = 0 Ω	5.0		7.0				pC
			3.3		3.0				pC
OIRR	Off Isolation (9)	Figure 4, R_L = 50 Ω , f = 10MHz	1.65 ~ 5.5		-57				dB
Xtalk	Crosstalk	Figure 5, R_L= 50 Ω , f = 10MHz	1.65 ~ 5.5		-54				dB
BW	−3 dB Bandwidth	Figure 8, R_L = 50 Ω	1.65 ~ 5.5		350M				Hz
THD	Total Harmonic Distortion (7)	R_L = 600 Ω, 0.5VP-P f = 600 Hz ~ 20 kHz	5.0		0.011				%
CIN	Select Pin Input Capacitance (10)		0		2.3				pF
CIO-B	B Port Off Capacitance (10)	Figure 6	5.0		5.0				pF
CIOA-ON	A Port Capacitance when Switch is Enabled (10)	Figure 7	5.0		15.5				pF

Note:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

4. Parameter is characterized but not tested in production.

5. Δ RON = RON max − RON min measured at identical VCC , temperature and voltage levels.

6. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

7. Guaranteed by Design.

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

9. Off Isolation = 20 log10 [VA/VBn].

10. TA = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

TEST CIRCUITS

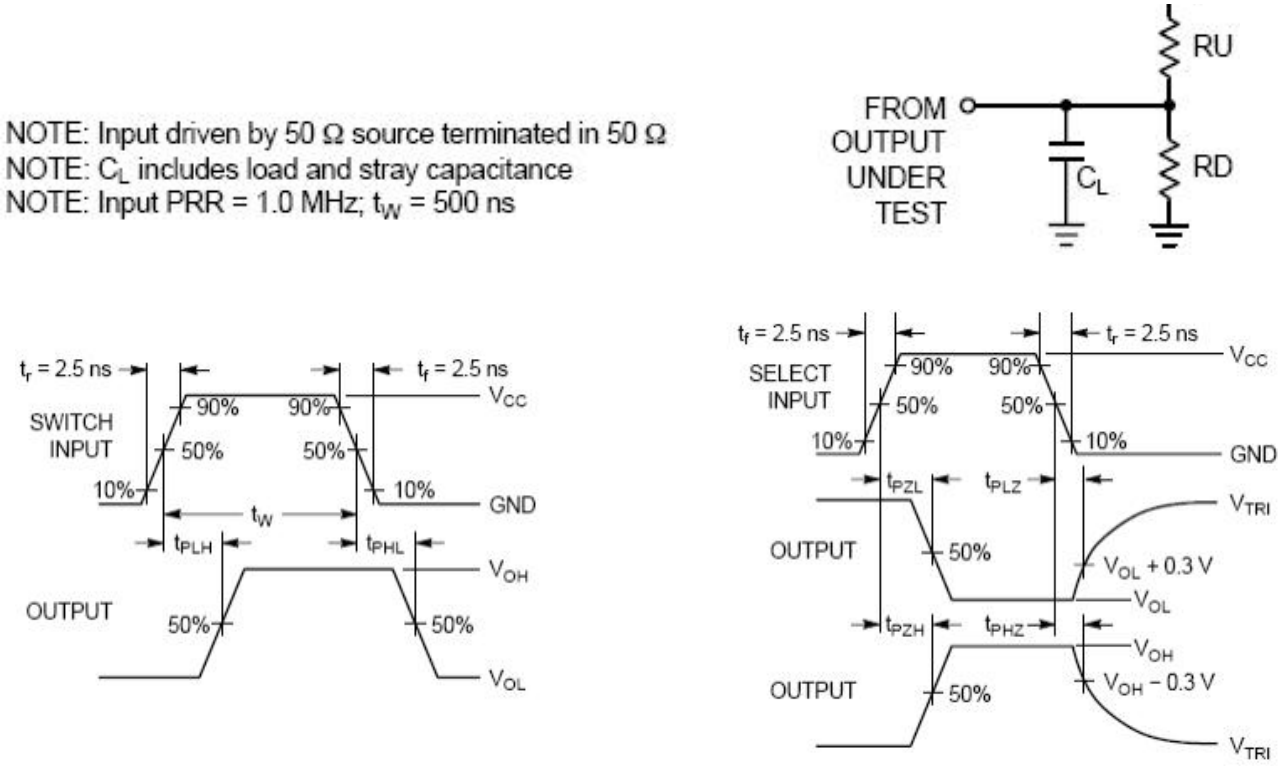


Figure 1. AC Test Circuit ,AC Waveforms

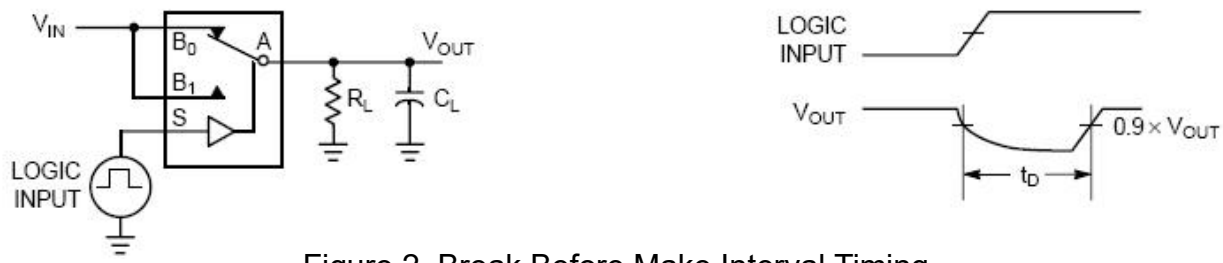


Figure 2. Break Before Make Interval Timing

TESTCIRCUITS(continued)

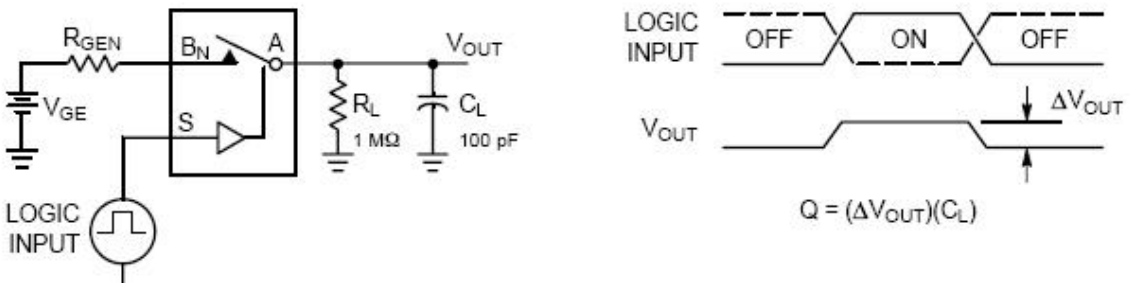


Figure 3. Charge Injection Test

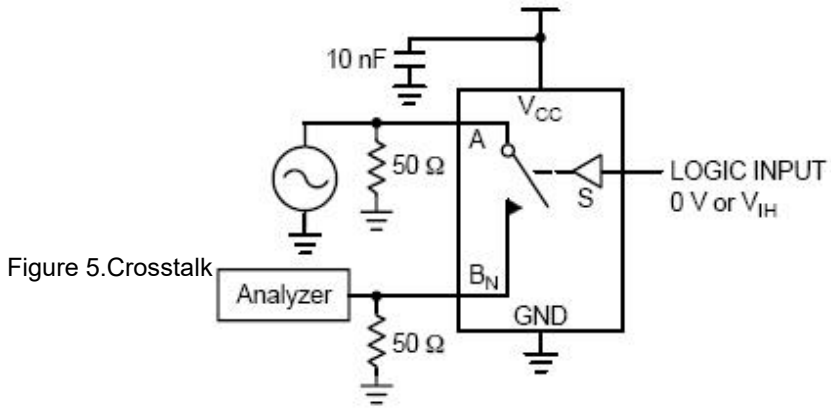


Figure 5.Crosstalk

Figure 4. Off Isolation

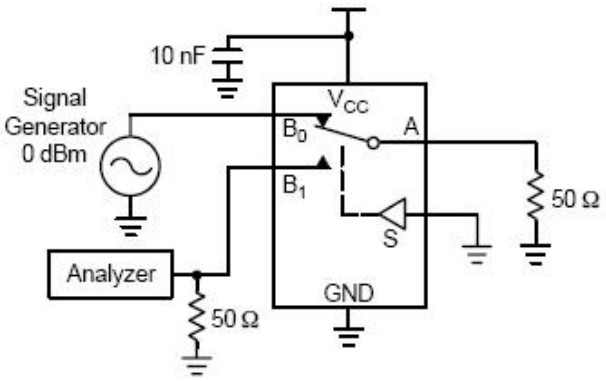


Figure 5.Crosstalk

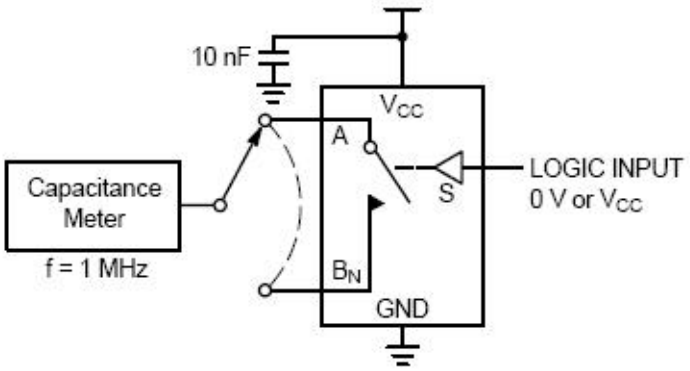


Figure 6. Channel Off Capacitance

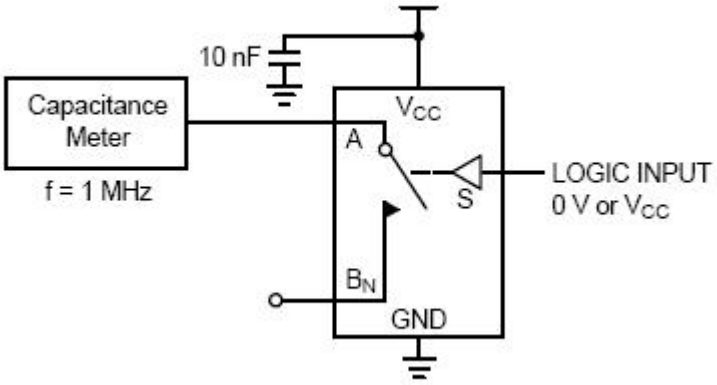


Figure 7. Channel On Capacitance

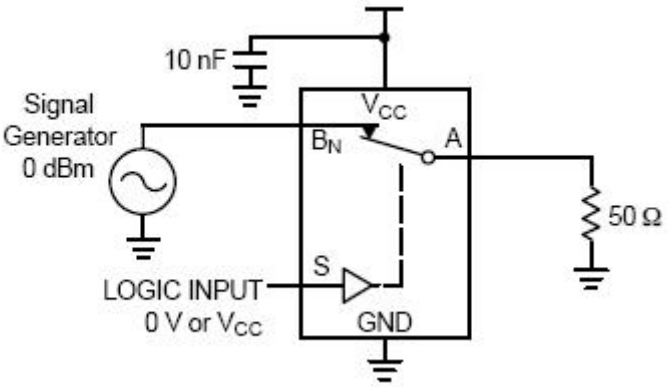
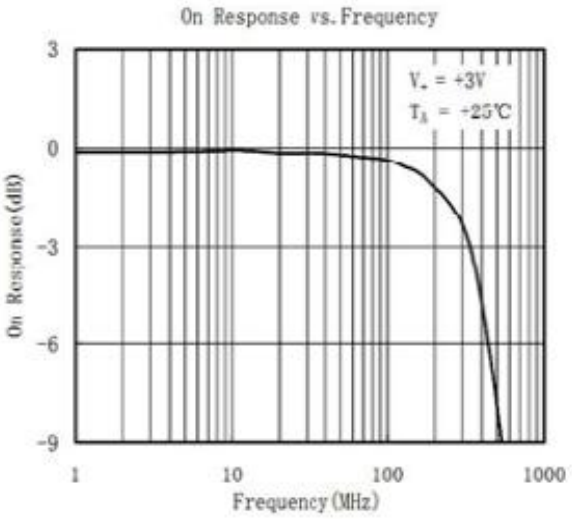
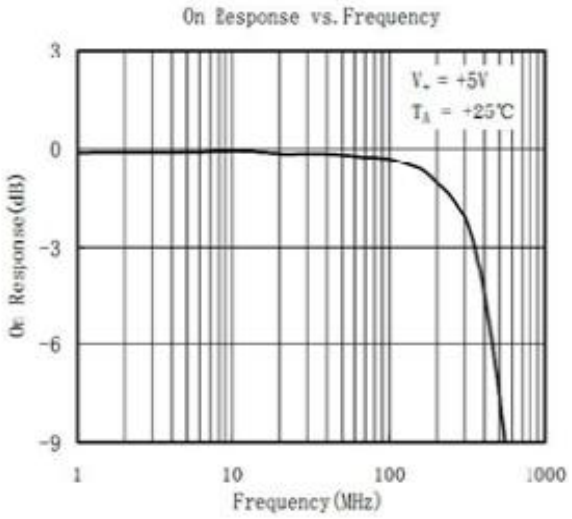
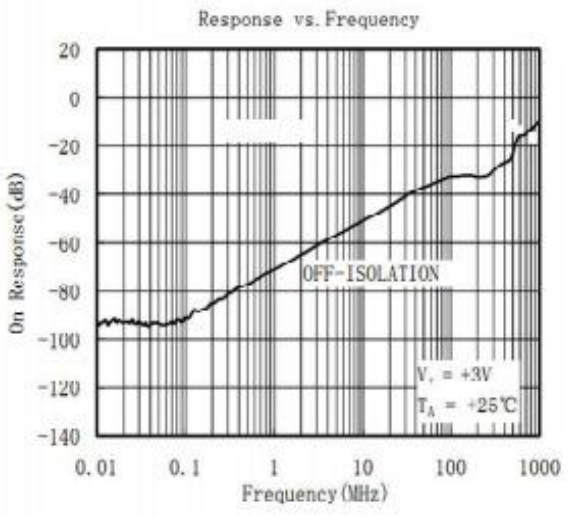
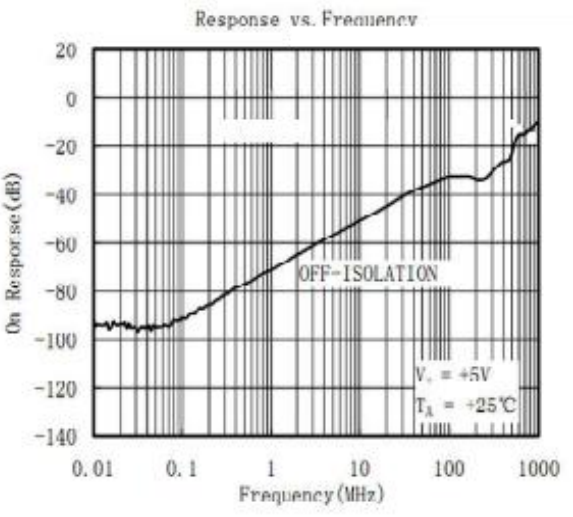


Figure 8. Bandwidth


On Response vs. Frequency
3
0
-3
-6
-9
On Response (dB)
1
10
100
1000
Frequency (MHz)
V+ = +3V
TA = +25℃

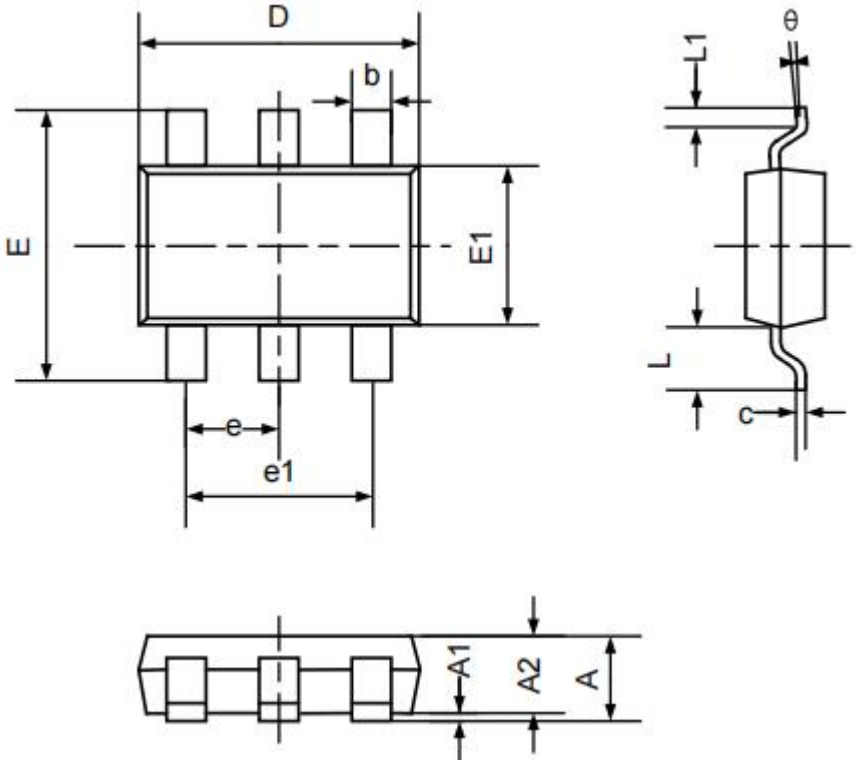

On Response vs. Frequency
3
0
-3
-6
-9
On Response (dB)
1
10
100
1000
Frequency (MHz)
V+ = +5V
TA = +25℃


Response vs. Frequency
20
0
-20
-40
-60
-80
-100
-120
-140
On Response (dB)
0.01
0.1
1
10
100
1000
Frequency (MHz)
OFF-ISOLATION
V+ = +3V
TA = +25℃


Response vs. Frequency
20
0
-20
-40
-60
-80
-100
-120
-140
On Response (dB)
0.01
0.1
1
10
100
1000
Frequency (MHz)
OFF-ISOLATION
V+ = +5V
TA = +25℃

PACKAGE OUTLINE

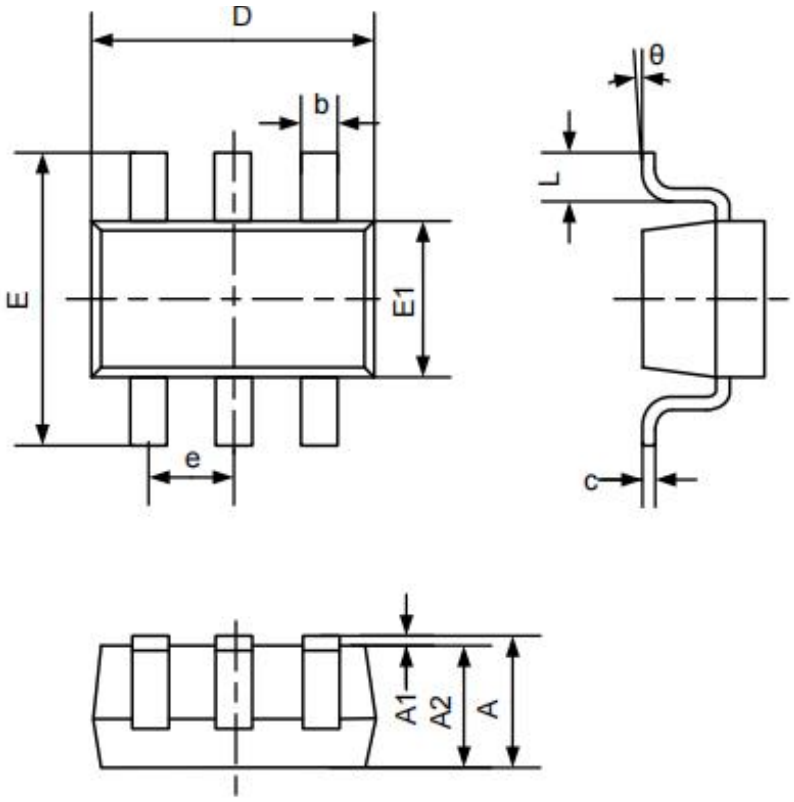
SC70-6



Symbol	Dimensions in Millimeters	
	Min	Max
A	0.85	1.05
A1	0.00	0.10
A2	0.80	1.00
b	0.15	0.35
c	0.08	0.22
D	2.02	2. 12
E	2.20	2.40
E1	1.25	1.35
e	0.65BSC	
e1	1.30BSC	
L	0.50REF	
L1	0.28	0.38
θ	0°	8°

PACKAGE OUTLINE

SOT-23-6



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A			1.240
A1	0.010	0.050	0.090
A2	1.050	1.100	1.150
b	0.300	0.350	0.400
c	0.117		0.157
D	2.870	2.920	2.970
E	2.720	2.800	2.880
E1	1.550	1.600	1.650
e	0.950BSC		
1	1.900BSC		
L	0.320	0.400	0.480
θ	0°		5°