General Description

This single 3-input positive-NAND OR gate is designed for 1.65-V to 5.5-V VCC operation.

The SN74LVC1G10 device performs the Boolean function $Y=A \cdot B \cdot \overline{C}$ or $Y=\overline{A+B+C}$ in positive logic.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, prevents damaging current backflow through the device when it is powered down .

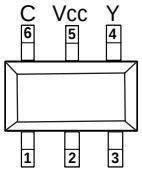
Features

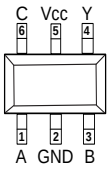
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Provides down translation to V_{CC}
- Low power consumption, 10-μA Max I_{CC}
- ±24-mA output drive at 3.3 V
- I_{off} supports live insertion, partial-power-down mode, and back drive protection

Applications

- AV receivers
- DLP front projection system
- Digital picture frames
- Digital radio
- Digital still cameras
- Digital video cameras (DVC)
- GPS: personal navigation devices
- Handset: smartphones
- Notebook PC and netbooks
- Network-attached storage (NAS)
- Power line communication modems
- Server PSU
- STB, DVR, and streaming media

Reference News

Pinning and Package	Marking
	

Pinning and Package	Marking
	

Pin Functions

Pin		I/O	Description
Name	SOT23-6/SC70-6		
A	1	I	Data Input
GND	2	-	Ground
B	3	I	Data Input
Y	4	O	Data Output
VCC	5	-	Supply Voltage
C	6	I	Data Input

Order information

Orderable Device	Package	Packing Option
SN74LVC1G10DBVR	SOT23-6	3000PCS
SN74LVC1G10DCKR	SC70-6	3000PCS

Absolute Maximum Ratings

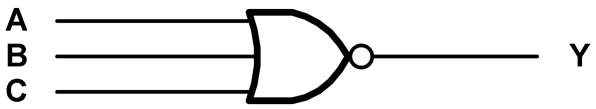
Parameters			Min	Max.	Unit
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range		-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2)(3)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
Continuous current through V_{CC} or GND				±100	mA
T_J	Junction temperature under bias			85	°C
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed

Functional Block Diagram



ESD Ratings

ESD			Value	Unit
V(ESD)	Electrostatic Discharge	Human-Body Model (HBM)(1)	8 K	V
		Charged-Device Model (CDM)(2)	2 K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	1.65	5.5	V
V_{IH}	High-Level Input Voltage	V_{CC}=1.65V to 1.95V	0.65×V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7×V_{CC}		
V_{IL}	Low-Level Input Voltage	V_{CC}=1.65V to 1.95V		0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3×V_{CC}	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-Level Output Current	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
I_{OL}	Low-Level Output Current	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Δt/Δv	Input Transition Rise or Fall Rate	V_{CC}=1.8V±0.15V, 2.5V±0.2V		20	ns/V
		V_{CC}=3.3V±0.3V		10	
		V_{CC}=5V±0.5V		5	
TA	Operating Free-air Temperature	All Other Packages	-40	125	°C

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-6	196	81	°C/W
SC70-6	178	98	°C/W

Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	V_{CC}	–40°C to 85°C			–40°C to 125°C			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{OH}		I_{OH}=–100 μA	1.65 V to 5.5 V	V_{CC}-0.1			V_{CC}-0.1			V
		I_{OH}=–4 mA	1.65 V	1.2			1.2			
		I_{OH}=–8 mA	2.3 V	1.9			1.9			
		I_{OH}=–16 mA	3V	2.4			2.4			
		I_{OH}=–24 mA		2.3			2.3			
		I_{OH}=–32 mA	4.5 V	3.8			3.8			
V_{OL}		I_{OL}=100 μA	1.65 V to 5.5 V			0.1			0.1	V
		I_{OL}=4 mA	1.65 V			0.45			0.45	
		I_{OL}=8 mA	2.3 V			0.3			0.3	
		I_{OL}=16 mA	3V			0.4			0.4	
		I_{OL}=24 mA				0.55			0.55	
		I_{OL}=32 mA	4.5 V			0.55			0.55	
I_I	A or B or C Inputs	V_I=5.5 V or GND	0 to 5.5 V			±5			±5	μA
I_{off}		V_I or V_O=5.5 V	0			±10			±10	μA
I_{CC}		V_I=5.5 V or GND, I_O=0	1.65 V to 5.5 V			10			10	μA
ΔI_{CC}		One Input at V_{CC} – 0.6 V, Other Inputs at V_{CC} or GND	3 V to 5.5 V			500			500	μA
C_i		V_I=V_{CC} or GND	3.3 V		4			4		pF

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Switching Characteristics, CL=15pF

Over recommended operating free-air temperature range (unless otherwise noted)

Parameter	From (Input)	To (Output)	–40°C to 85°C								Unit
			V_{CC}=1.8 V ± 0.15 V		V_{CC}=2.5 V ± 0.2 V		V_{CC}=3.3 V ± 0.3 V		V_{CC}=5 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
tpd	A or B or C	Y	2.6	15.2	1.6	5.6	1.2	4.1	1	3.1	ns

Over recommended operating free-air temperature range, CL=30 pF or 50 pF (unless otherwise noted)

Parameter	From (Input)	To (Output)	–40°C to 85°C								Unit
			V_{CC}=1.8 V ± 0.15 V		V_{CC}=2.5 V ± 0.2 V		V_{CC}=3.3 V ± 0.3 V		V_{CC}=5 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
tpd	A or B or C	Y	2.9	17.2	1.4	6.2	1.3	4.9	1	3.5	ns

Over recommended operating free-air temperature range, CL=30 pF or 50 pF (unless otherwise noted)

Parameter	From (Input)	To (Output)	–40°C to 125°C								Unit
			V_{CC}=1.8 V ± 0.15 V		V_{CC}=2.5 V ± 0.2 V		V_{CC}=3.3 V ± 0.3 V		V_{CC}=5 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
tpd	A or B or C	Y	2.9	20	1.4	7.8	1.3	6.2	1	4.6	ns

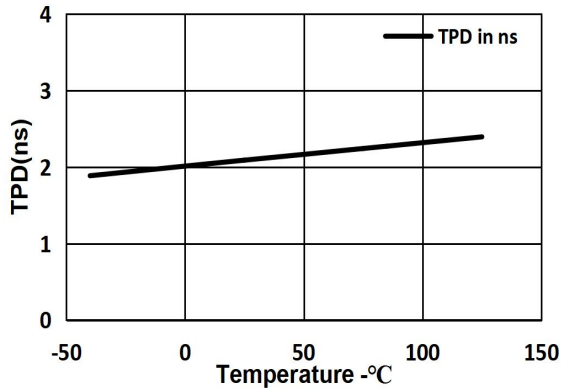
Operating Characteristics

TA=-40°C to +125°C

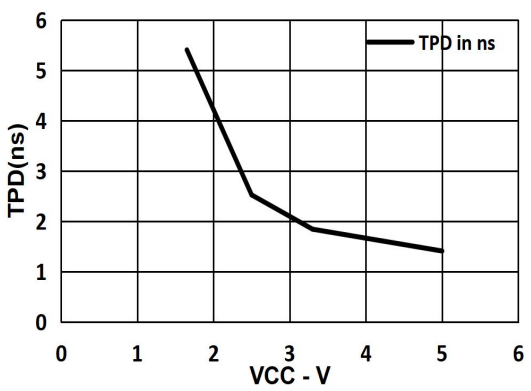
Parameter		Test Conditions	V_{CC}=1.8V	V_{CC}=2.5V	V_{CC}=3.3V	V_{CC}=5V	Units
			Typ	Typ	Typ	Typ	
C_{pd}	Power Dissipation Capacitance	f=10Mhz	18	19	20	23	pF

Typical Characteristics

V_{CC}=1.65V or 5.5V, FULL=–40°C to +125°C. Typical values are at TA=+25°C (unless otherwise noted)

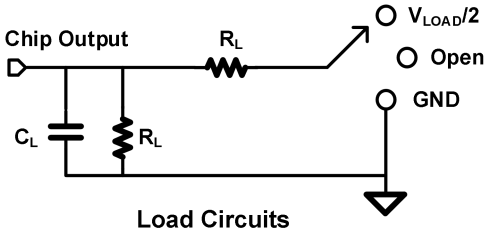


TPD Across Temperature at 3.3V V_{CC}



TPD Across V_{CC} at 25℃

Parameter Measurement Information

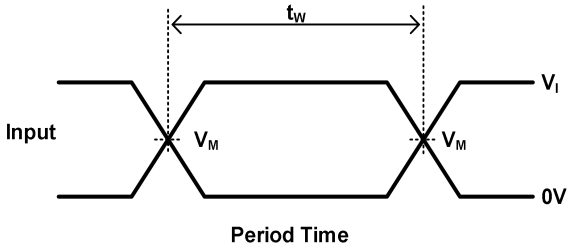


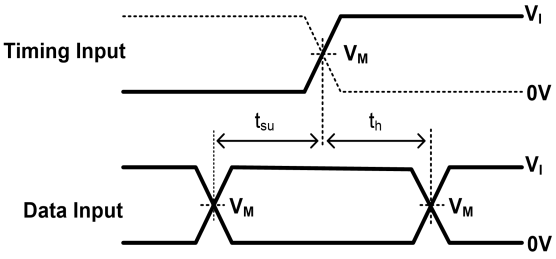
Load Circuits

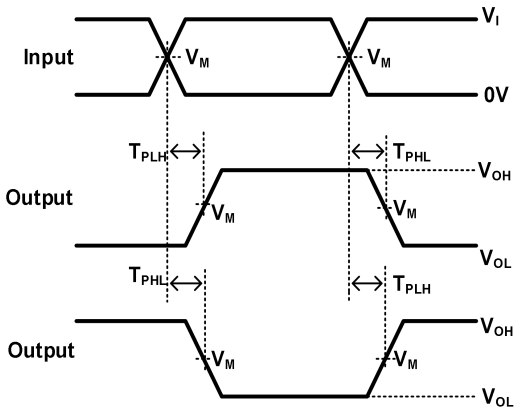
TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	15pF	1MΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	15pF	1MΩ	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	15pF	1MΩ	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	2×V_{CC}	15pF	1MΩ	0.3V

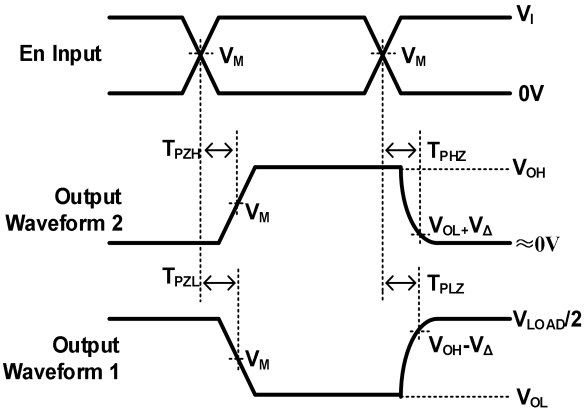
Parameter Measurement Information(Continued)







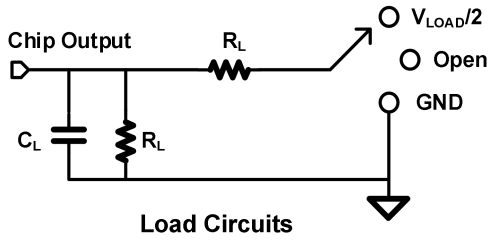
Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

Notes: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50 .
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all devices.

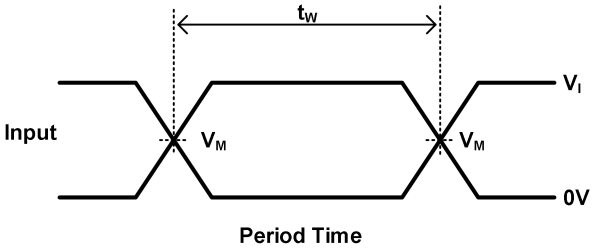
Parameter Measurement Information(Continued)



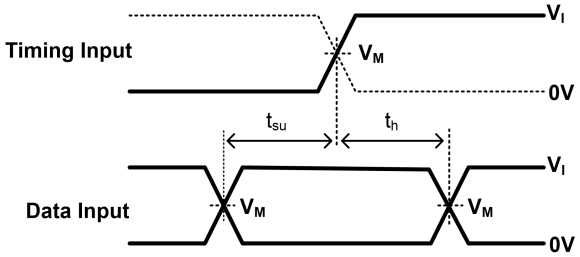
Load Circuits

TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

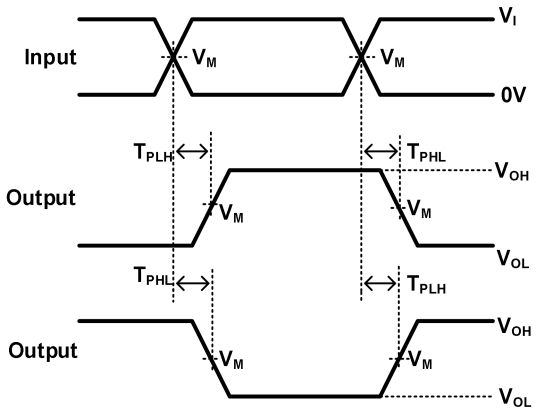
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	1kΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	500Ω	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	50pF	500Ω	0.3V



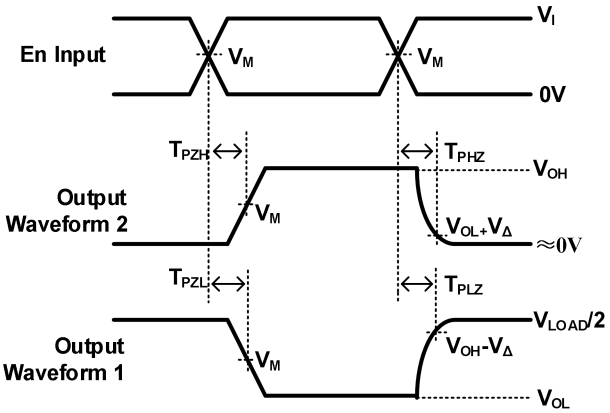
Period Time



Setup and Hold Times



Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

Notes: A. C includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z=50.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all device.

Detailed Description

This 3-input NAND gate is designed for 1.65-V to 5.5-V V_{CC} operation. The SN74LVC1G10 device features a three-input NAND gate. The output state is determined by eight patterns of 3-bit input. All inputs can be connected to V_{CC} or GND. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Feature Description

- Wide operating voltage range.
- Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

Device Functional Modes

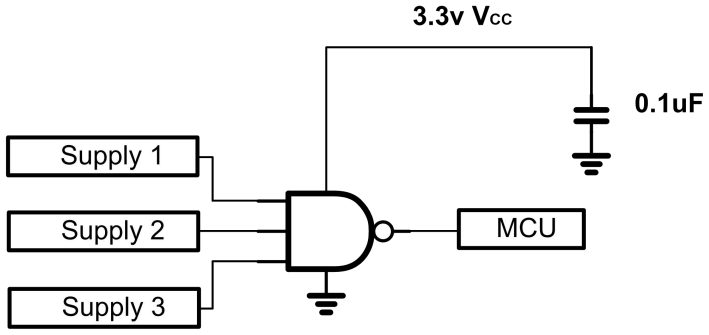
Input A			Output
A	**B**	**C**	**Y**
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

ApplicationInformation

The SN74LVC1G10 device offers logical NAND configuration for many design applications.

This example describes basic power sequencing using the NAND gate configurationPower sequencing is often used in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. In the application below, the power-good signals from the supplies tell the MCU to continue an operation.

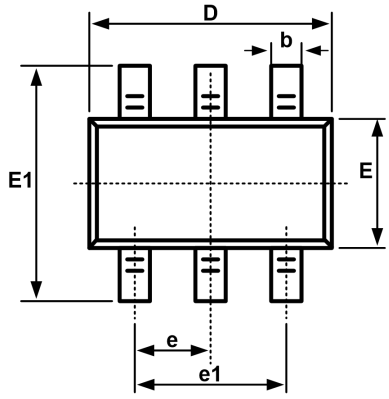
Typical Application

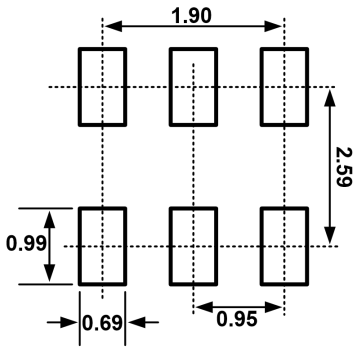


Typical Application Diagram

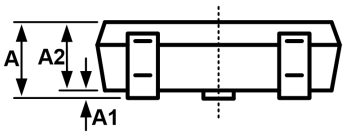
Package Outline

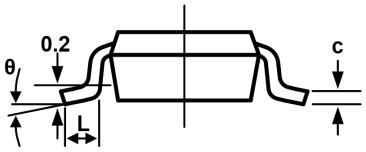
SOT23-6





Recommended Land Pattern (Unit: mm)

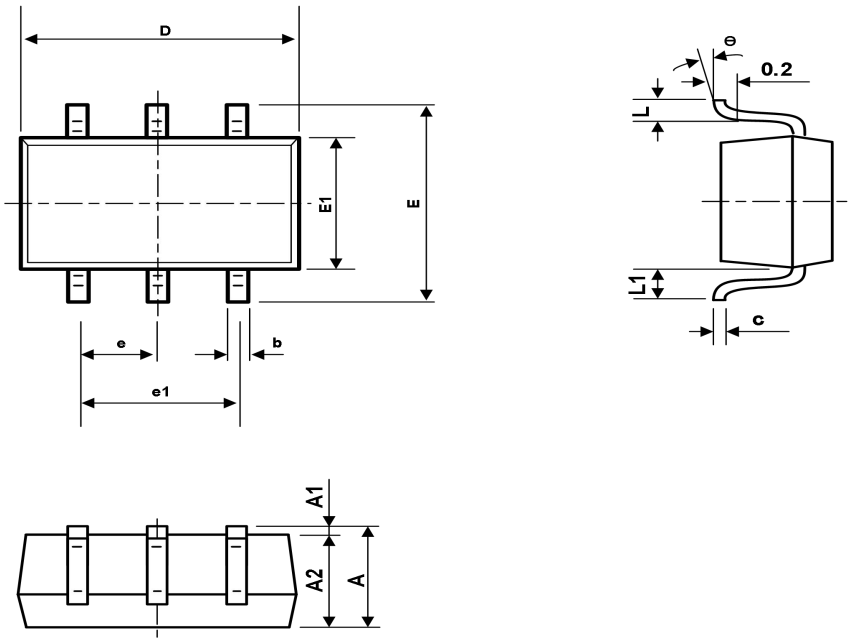




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950BSC		0.037BSC	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF		0.024REF	
θ	0°	8°	0°	8°

Package Outline

SC70-6



Symbol	Dimension In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.	1.	0.	0.
A1	9000.	1000.	0350.	0430.
A2	0000.	1001.	0000.	0040.
b	9000.	0000.	0350.	0390.
c	1500.	3500.	0060.	0140.
D	1102.	1752.	0040.	0070.
E	0002.	2002.	0790.	0870.
E1	1501.	4501.	0850.	0960.
e	0.650TYP		0.026TYP	
e1	1501.	3501.	0450.	0530.
L	2000.	4000.	0470.	0550.
L1	260	0.525REF 460	010	0.021REF 018
θ	0°	8°	0°	8°